

Memory Controllers

- The MBC-5 Memory Controller IC has been manufactured for the purpose of memory management. All Game Boy Color games should be produced using the MBC-5 memory controller.

MBC-5 Instructions

MBC-5 supports high speed mode for DMG (Game Boy), MGB (Game Boy Pocket), MGL (Game Boy Light), SGB (Super Game Boy), SGB2 (Super Game Boy 2), henceforth all referred to as DMG, as well as CGB (Game Boy Color).

Maximum ROM size 64 Mbit (512 banks in units of 128 Kbit).

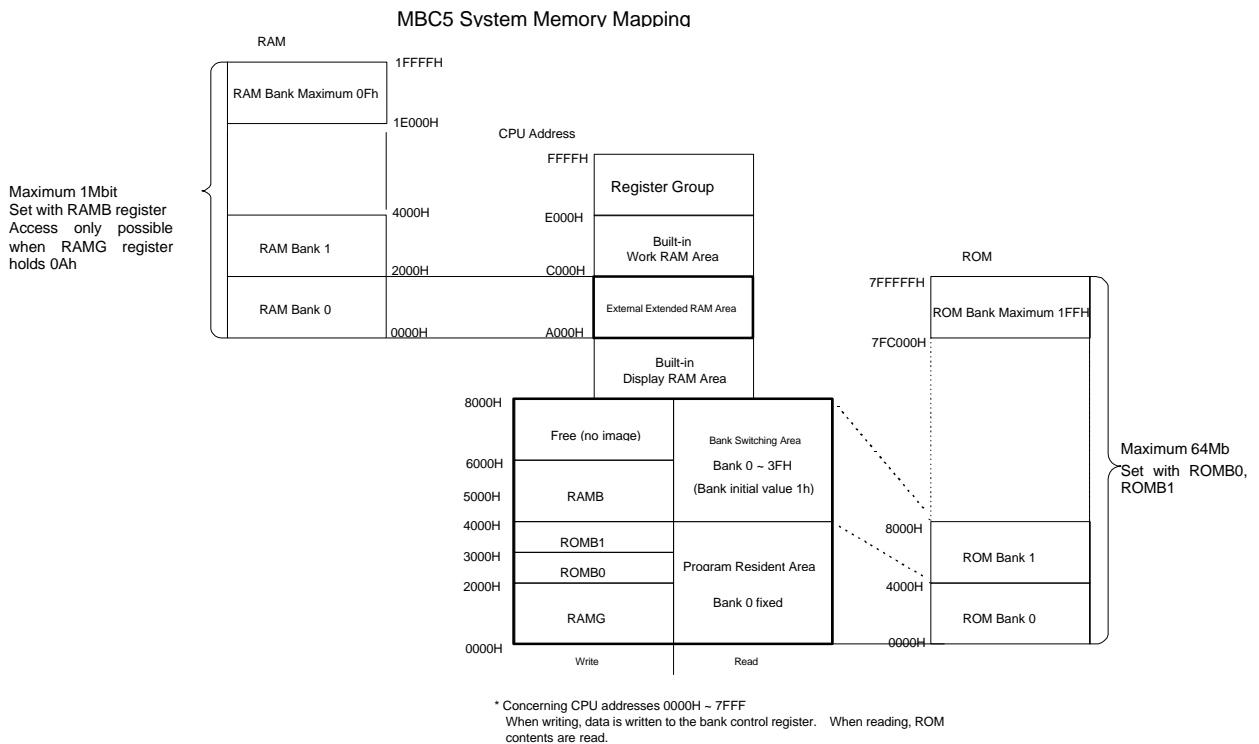
Maximum RAM size 1 Mbit (16 banks in units of 64 Kbit).

NOTE: MBC-5 is MBC-1 upward compatible.

Register Table

Name	Address (h)
RAMG	0000 ~ 1FFF
ROMB0	2000 ~ 2FFF
ROMB1	3000 ~ 3FFF
RAMB	4000 ~ 5FFF

Memory Map



Explanation of Registers

External Extended Memory Register (RAMG)

This register enables/disables access to external extended RAM. Access to external extended RAM is enabled by writing 0Ah in the RAMG register space from 000h to 1FFFh. If anything other than 0Ah is in this register, then read and write to RAM is disabled.

Bit	7	6	5	4	3	2	1	0
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Initial value	0	0	0	0	0	0	0	0
R/W					W			

Lower ROM Bank Register (ROMB0)

This register sets the lower 8 bits of the 9-bit ROM bank register. The ROM bank can be changed by writing the desired ROM bank number in the ROMB0 register, which is the area from 2000h to 2FFFh.

Bit	7	6	5	4	3	2	1	0
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Initial value	0	0	0	0	0	0	0	0
R/W					W			

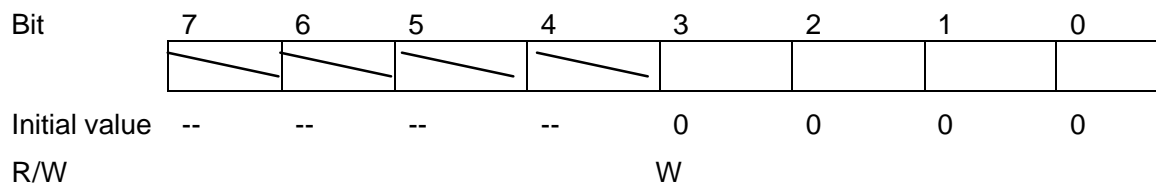
Upper ROM Bank Register (ROMB1)

This register sets the upper 1 bit of the 9-bit ROM bank register. The ROM bank can be changed by writing the desired ROM bank number in the ROMB1 register, which is the area from 3000h to 3FFFh.

Bit	7	6	5	4	3	2	1	0
	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Initial value	--	--	--	--	--	--	--	0
R/W								W

RAM Bank Register (RAMB)

This register sets the RAM bank register. The RAM bank can be changed by writing the desired RAM bank number in the RAMB register, which is the area from 4000h to 5FFFh.



Note: Bits that are crossed out are ignored by MBC5, but please use them as "0." The initial values are the values that are set automatically when the power is turned on and the system reset.

MBC-5 Programming Cautions

Changing from MBC1 to MBC5

Selecting ROM Banks

If addresses between 3000h and 3FFFh are used for register 1 (ROM bank control) in your MBC1 program, then MBC5 will not be able to select the ROM bank as intended by ROMB1. So please use an area between 2000h ~ 2FFFh for register 1 in your MBC1 program. In MBC1 programs of more than 8 Mbits, register 2 (the ROM or RAM bank control register) is used in the ROM upper bank. Be careful, because in the case of MBC5, the RAM bank will change but the ROM bank will stay the same.

ROM banks 20, 40, 60h

MBC1 cannot use 20, 40, 60h ROM banks, but MBC5 can.

Register 3 of MBC1 (ROMRAM select)

Because ROM and RAM addresses are independent in MBC5, there is no need for the ROMRAM select. A write instruction to set register 3 left over in a program for MBC1 will be ignored and have no effect on MBC5.

General Notes of Caution

Memory Image

When a memory device with less than the maximum built-in memory capacity (ROM: 64 Mbit, RAM: 1Mbit) is used, memory images will be generated in the free bank areas. Since this can cause problems, please do not develop software which use images.

Protecting RAM Data


In order to protect RAM data, we recommend that you disable RAM (RAMG = 00h) whenever RAM is not being accessed.

Examples of MBC5 programs with DMG, CGB

Setting Bank Switching Area (4000h ~ 7FFFh) to ROM Bank 1FFh

```
LD A,$FF
LD ($2000),A ; Set ROMB0
LD A,$01
LD ($3000),A ; Set ROMB1
|
|
|
```

Setting External Extended Memory Area (A000h ~ BFFFh) to RAM Bank Fh and Accessing the Area

```
LD A,$0F
LD ($4000),A ; Set RAMB
LD A,$0A
LD ($0000),A ; Enable access to RAM
|            RAM access process
|
|
LD A,$00
LD ($0000), A ; Prohibit access to RAM
```